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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AHMED, HAMDY S	
ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,427	VERDUN, GARY J.	
	Examiner	Art Unit	
	HAMDY S. AHMED	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, and 4-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114

Claim 3 is cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, and 4-23 under 35 U.S.C. 102(e) as being anticipated by Schuckle et al. (US No.: 7017054 B2).

As to claim 1, Schuckle hereinafter teaches, a computer system (see column 2, line 65), comprising: a processor (see column 2, line 60); a cache associated with the processor (see column 2, line 60); system memory (see column 3, line 29); a write tracking buffer external to the processor (each cache has a buffer for write back and updating the cache, and it is external to the processor; the index is acting like a buffer; see column 7, line 1); wherein the write tracking buffer is maintained a memory controller hub that is operable to tracing buffer bus master operable to access system memory (see figure 1 where the processor is the control device that control the operation of the memory system , which is operable to hub of the main memory, using the bus master which is element 180); wherein the write tracing is operable to hold as entries the addresses of writes to system memory (see columns7, lines 1 - 3) during the

period that processor is in a low power state (see column 5, lines 6); and wherein the processor is operable to invalidate the lines of cache corresponding to the entries of the write tracking buffer (see column 6, lines 45 - 48) upon the processor exiting its low power state (see column 7, lines 20 - 21).

As to claim 2, the Schuckle reference teaches the low power state (i.e. the Deep Sleep) of the processor (see column 6, line 1) that comprises a non-snoopable state (when the processor in C3 or C2 as in column 6, line 17, because C1 is defined as snoopable; see column 6, line 50), be in which the processor is not able to monitor accesses to system memory (see column 5, lines 66 - 67).

As to claim 4, the Schuckle reference teaches the cache that is an internal processor cache (see column 7, lines 9 - 10).

As to claim 5, the Schuckle reference teaches a method for managing the power consumption (see column 2, lines 6 - 7) by a processor (see column 2, line 2) in a computer system (see column 2, line 8), the computer system including system memory (see column 3, line 29) and the processor including an internal cache (see column 3, line 2), comprising the steps of: causing the processor to enter a low power state (see column 2, lines 5 - 6); during the period that the processor is in a low power state, writing in a buffer external to the processor the addresses of modified data in system memory (see column 3, lines 9 - 10); where the buffer is is maintained a memory controller hub that is operable to tracing buffer bus master operable to access system memory (see figure 1 where the processor is the control device that control the operation of the memory system , which is operable to hub of the main memory, using the bus master which is element 180) , and upon the processor exiting the low power state (see column 3, lines 6 - 10), invalidating those lines that correspond to the memory addresses recorded in the buffer (see column 6, lines 45 - 56).

As to claim 6, Schuckle reference teaches a method further comprising the step of invalidating the content of the buffer (see column 6, lines 45 - 56, because each cache contains a buffer).

As to claim 7, Schuckle reference teaches a method wherein the step of causing the processor to enter a low power state (see column 3, lines 17 - 18) comprises the step of causing the processor to enter a low power state in which the processor is unable to perform the task of snooping (see column 3, lines 20 - 21) accesses by bus masters to system memory (see column 5, lines 45 - 46).

As to claim 8, the Schuckle reference teaches the method wherein the step of writing to the buffer the addresses of modified data in system memory comprises the step of writing to the buffer the address of each block of memory modified by a bus master (see column 3, lines 9 - 13, because the buffer is included in the cache) of the computer system (see column 3, line 27) during the period the processor is in the low power state (see column 3, lines 10 - 11).

As to claim 9, the Schuckle reference teaches the method wherein the step of writing to the buffer the addresses of modified data in system memory (see column 3, lines 9 - 13, because the buffer is included in the cache) of the computer system (see column 3, line 27) comprises the step of writing the address to the buffer only if it is determined that the address has not already been written to the buffer (all the addresses of memory locations are stored in the index (i.e., buffer), (See column 7, lines 1 - 3).

As to claim 10, the Schuckle reference teaches a method that further comprises the step of causing the processor to exit its low power state once the buffer is full (for the processor to exit its low power state, depending on the status of the cache line, which inherently contains a buffer; see column 10, lines 34 - 37).

As to claim 11, the Schuckle reference teaches a method further comprising the step of, before causing the processor to enter the low power state (see column 10, lines 28 - 33), writing to system memory the content of those lines of the cache (see column 10, lines 9 - 11) that have been modified relative to the content of the corresponding locations in system memory (see column 10, lines 64 - 66).

As to clam 12, the Schuckle reference teaches a method for managing cache coherency in an formation handling system (see column 7, lines 6 - 8), the information handling system including a processor (see column 7, line with an internal cache (see column 7, line 4) and system memory (see column 7, line 1 and line 12), comprising the steps of: performing a write back operation to write to system memory those cache lines that have been modified relative to the content of corresponding memory locations in system memory (See column 11, lines 54 - 57) ; causing the processor to enter a low power state (see column 5, lines 6); during the period that the processor is in a low power state (see column 11, lines 59 - 60), writing in a buffer external to the processor (the buffer is in the cache, and the cache is outside the processor) the addresses of data in system memory that have been modified (see column 10, lines 64 - 66) by a bus master (the bus master is driven by the memory controller, see column 5, line 46) in the information handling system; where the buffer is maintained in memory controller hub (this system include a network controller that provide an information handling system as in column 8 lines 16-30 a buffer should be included inherently) that as in and upon the processor exiting the low power state for a higher power state (see column 5, lines 46 - 47), invalidating in the cache those cache lines corresponding to the memory addresses recorded in the buffer (see column 6, lines 45 - 46).

As to claim 13, the Schuckle reference teaches a method further comprising the step of cleaning the buffer following the step of invalidating the cache lines corresponding to the memory addresses recorded in the buffer (see column 5, lines 45 - 49).

As to claim 14, Schuckle reference teaches a method further comprising the step of following the step of invalidating cache lines corresponding to memory addresses recorded in the buffer (see column 6, lines 45 - 46), writing to the invalidated cache lines the content of the corresponding memory addresses in system memory (see column 5, lines 45 - 49).

As to claim 15, the Schuckle reference teaches a method wherein the step of writing to the buffer comprises the step of writing to the buffer only if it is determined that the address of the modified memory location has not been previously recorded in the buffer (see column 10, lines 58 - 67).

As to claim 16, the Schuckle reference teaches the method further comprising the step of causing the processor to exit its low power state for a higher power state upon a determination that the buffer is full (see column 5, lines 46 - 47).

As to claim 17, the Schuckle reference teaches an information handling system (see column 2, lines 6 - 7), comprising: a processor having an internal processor cache (see column 7, line 4); system memory (see column 10, line 41); a buffer (the cache inherently contains a buffer); a memory controller (see column 3, line 6); wherein the memory controller (see column 3, line 6) is operable to populate the buffer with the addresses of writes made to system memory during the period that the processor is in a low power state (see column 3, lines 6 - 9); and wherein the buffer is maintained in the memory controller, (this system include a network controller that provide an information handling system as in column 8 lines 16-30 a buffer should be included inherently) and wherein the processor, upon exiting the low power state (see

column 3, lines 9 - 10), is operable to invalidate cache lines of the processor cache corresponding to the addresses recorded in the buffer (the cache inherently contains a buffer).

As to claim 18, the Schuckle reference teaches the system wherein the low power state is a non-snoopable state characterized by the inability (see column 3, lines 20 - 21) of the processor to monitor writes to system memory by a bus master of the information handling system (see column 10, lines 4 - 11).

As to claim 19, the Schuckle reference teaches the system wherein the memory controller is operable to cause the processor to exit its low power state when the buffer is full (for the processor to exit its low power state, depending on the status of the cache line, which inherently contains a buffer; see column 10, lines 34 - 37).

As to claim 20, Schuckle reference teaches, wherein the processor is operable to perform, before entering a low power state (see column 3, lines 14 - 17), a write-back operation to system memory in which all modified cache lines are written to the corresponding locations in system memory (See column 11, lines 54 - 57).

As to claim 21, the Schuckle reference teaches a method for managing cache coherency in a computer system (see column 7, lines 7 - 9) following the entry of a processor into a low power state (see column 7, lines 30 - 31), the computer system (see column 3, line 27) including a processor having an internal cache (see column 3, line 2), system memory (see column 3, line 29), and an external write tracking buffer operable to store the addresses of system memory addresses modified during the period that the processor was in the low power state (see column 7, lines 1 - 3 in which the index is a buffer), wherein the write tracking buffer is maintained a memory controller hub that is operable to tracing buffer bus master operable to access system memory (see figure 1 where the processor is the control device that control the operation of the memory system , which is operable to hub of the main memory, using the bus master which is

element 180) comprising the steps of: causing the processor to exit the low power state (see column 3, lines 9 - 10); and invalidating in the internal cache those cache lines corresponding to the memory addresses stored in the buffer (see column 6, lines 45 - 48).

As to claim 22, the Schuckle reference teaches the method further comprising the step of clearing the buffer following the step of invalidating cache lines in the internal cache (see column 6, lines 45 - 56, because each cache contains a buffer).

As to claim 23, the Schuckle reference teaches the method further comprising the step of following the step of invalidating cache lines corresponding to memory addresses stored in the buffer, writing to the invalidated cache lines the content of the corresponding memory addresses in system memory (see column 6, lines 45 - 56, because each cache contains a buffer).

Response To Arguments

With regard to the first argument, Schuckle discloses clearly, a memory controller hub (see figure 1 where the processor is the control device that control the operation of the memory system, which is operable to hub of the main memory). With regard to second argument Schuckle discloses, a buffer for storing the modified data during the period that the processor in low power state (this system teaches, when the processor in low state and high state, a buffer has to exist in the memory controller so, that the value after determination is made in which state the processor in, can be stored, inherently).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hamdy S. Ahmed whose telephone number is 571-270-1027. The examiner can normally be reached on M-TR 7:30-5:00pm and Every 2nd Friday 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hung Sough can be reached on 571-272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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2/15/08

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